CSP MOSFET 数据手册

NP12055ECC

CSP 12V Typ 4.9mΩ Dual N-Channel MOSFET

Rev 1.0

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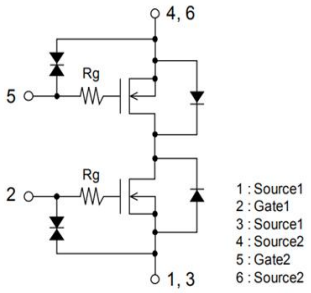
CSP 12V Typ 4.9mΩ Dual N-Channel NP12055ECC

产品特性 Features

- 2.5V 驱动电压 2.5 V Drive
- 共漏极结构，设计方便 Common-Drain Configuration for Design Simplicity
- 低的导通电阻 Low Source-Source ON Resistance
- 2kV HBM 栅极静电保护 2kV HBM ESD Diode-Protected Gate
- 无铅引脚，无卤化符合 RoHS 要求 Pb-Free, Halogen Free and RoHS Compliance
- 湿敏等级 1 MSL1

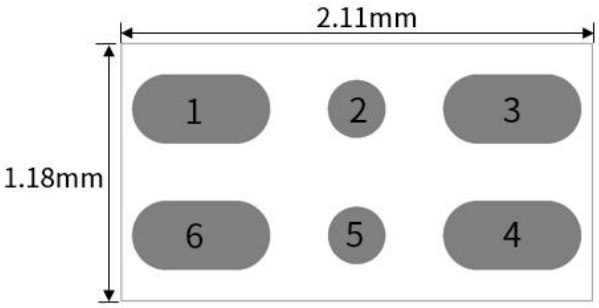


原理图
Schematic diagram

应用领域 Applications

- 单节锂电池充放电开关 1-Cell Lithium-ion Battery Charging and Discharging Switch
- 锂电池保护开关 Battery Protection Switch

关键参数与封装信息 Key Performance and Package Parameters



1,3:Source1(FET1)
2:Gate1 (FET1)
4,6:Source2(FET2)
5:Gate2(FET2)
Package Type:CSP
Size:2.11(mm)×1.18(mm)×0.30(mm)

产品型号 Part No.	封装 Package	源极到源极电压 V_{SS}	源极电流最大值 I_S Max	导通电阻 $R_{SS(on)}$	印记 Markin
NP12055ECC	CSP	12V	10.5A	4.9 mΩ@4.5 V	12055B
				5.3 mΩ@3.8 V	
				6.2 mΩ@3.1 V	
				7.6 mΩ@2.5 V	

最大额定值 Maximum Ratings①

参数 Parameter	符号 Symbol	数值 Value	单位 Unit
源极-源极击穿电压 Source-Source Breakdown Voltage	BV_{sss}	12	V
栅极-源极电压 Gate to Source Voltage	V_{GS}	±8	V
直流源极电流 Source Current (DC)	Is②	10.5	A
	Is③	17	A
脉冲源电极电流 Source Current (Pulse) PW≤10μs,Duty Cycle≤1%	Isp	105	A
单脉冲雪崩能量 Single Pulsed Avalanche Energy	EAS	80	mJ
耗散功率 Power Dissipation	P_D②	1.1	W
	P_D③	3.3	W
结温 Operating Junction Temperature	T_J	-55...+150	°C
存储温度 Storage Temperature	T_{stg}	-55...+150	°C

①超过最大额定值表中列出的使用条件可能会损坏芯片。如果超过这些限制值中的任何一个，则芯片的功能可能无法保证，芯片可能发生损坏并影响可靠性。

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

热阻特性 Thermal Resistance

参数 Parameter	符号 Symbol	数值（最大） Max. Value	单位 Unit
结到环境热阻 Thermal Resistance Junction to Ambient	$R_{\theta JA}$②	116	°C /W
	$R_{\theta JA}$③	38	°C /W

②芯片表面贴于 20mmX20mmXt1mm 环氧树脂基板。

Surface mounted on 20mmX20mm FR4 board

③芯片表面贴于 70mmX70mmXt1mm 陶瓷基板。

Surface mounted on 70mmx70mm FR4 board

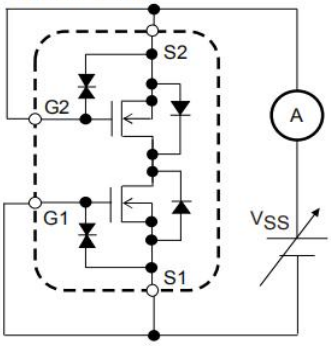
电气特性 Electrical Characteristics (T_J = 25°C unless otherwise noted)

项目③ Parameter	符号 Symbol	测试条件 Conditions	数值 Value			单位 Unit
			Min.	Typ.	Max.	
漏极-漏极击穿电压 Source to Source Breakdown Voltage	$V_{(BR)SSS}$	IS = 1 mA, VGS = 0 V Test Circuit 1	12	-	-	V
零栅压下漏极漏电流 Zero Gate Voltage Source Current	I_{SSS}	VSS = 10 V, VGS = 0 V Test Circuit 1	-	-	1.0	μA
栅极-漏极漏电流 Gate to Source Leakage Current	I_{GSS1}	VGS = ±5 V, VSS = 0 V Test Circuit 2	-	-	±1.5	μA
栅极-漏极漏电流 Gate to Source Leakage Current	I_{GSS2}	VGS = ±8 V, VSS = 0 V Test Circuit 2	-	-	±10	μA
阈值电压 Gate Threshold Voltage	$V_{GS(th)}$	VSS = 6 V, IS = 1 mA Test Circuit 3	0.4	-	1.0	V
漏极到漏极直流导通电阻 Static Source to Source On-State Resistance	$RSS_{(on)}$	IS =5 A, VGS = 4.5 V Test Circuit 4	3.0	4.9	5.9	mΩ
		IS =5 A, VGS = 3.8 V Test Circuit 4	4.0	5.3	7.8	mΩ
		IS =5 A, VGS = 3.1 V Test Circuit 4	4.5	6.2	8.2	mΩ
		IS =5 A, VGS = 2.5 V Test Circuit 4	5.0	7.6	9.8	mΩ
漏极到漏极正向压降 Forward Source to Source Voltage	VF(S-S)	IS=1A, VGS=0 Test Circuit 7	0.4	0.62	1.0	V
栅极电阻 Gate Resistance	Rg	f=1MHz	-	1500	-	Ω
输入电容 Input Capacitance	C_{iss}	VSS=10V VGS=0V f=1kHz	-	785	-	pF
输出电容 Output Capacitance	C_{oss}		-	660	-	pF
反向传输电容 Reverse Transfer Capacitance	C_{rss}		-	213	-	pF
开启延迟时间 Turn-On Delay Time	$t_{d(on)}$	TJ=25°C VSS =6V, ISS=5A, VGS=0/4.5V, RG=0Ω	-	0.04	-	μs
上升时间 Rise Time	t_r		-	0.35	-	μs
关断延迟时间 Turn-Off Delay Time	$t_{d(off)}$		-	8.1	-	μs
下降时间 Fall Time	t_f		-	12.6	-	μs

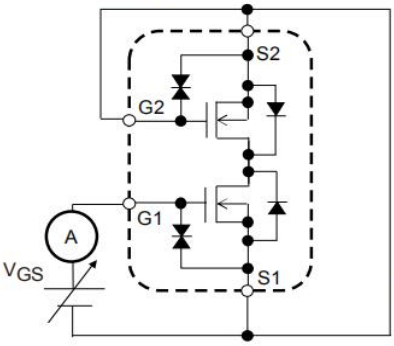
④产品的参数性能按照上述表格参数所描述，除非有额外的说明。如果产品工作在其他不同的条件下，产品的电学性能可能并不遵守上述参数。Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

测试电路范例 Test Circuits Example

Test Circuit 1
V_{SSS} / I_{SSS}

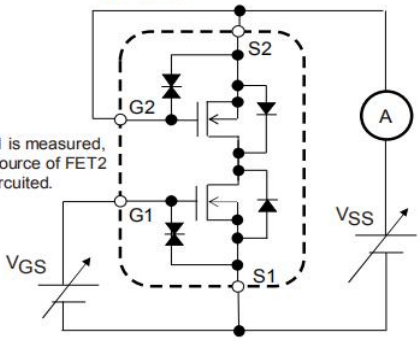


Test Circuit 2
I_{GSS}



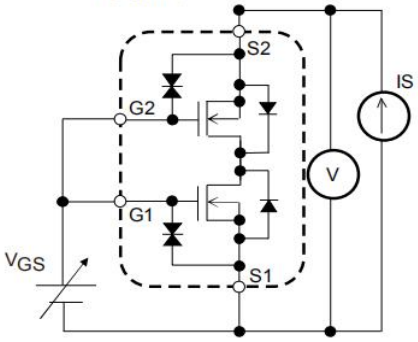
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 3
$V_{GS(th)}$

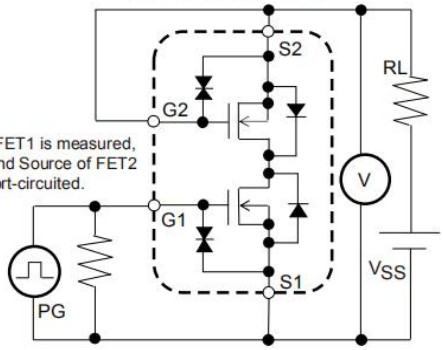


When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 4
$R_{SS(on)}$

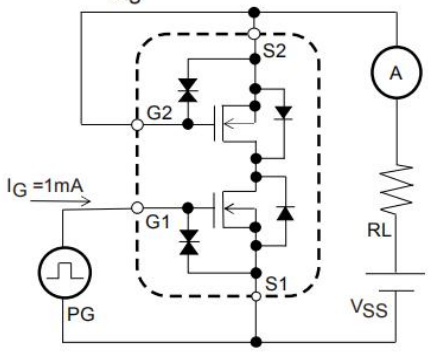


Test Circuit 5
$t_{d(on)}$, t_r, $t_{d(off)}$, t_f



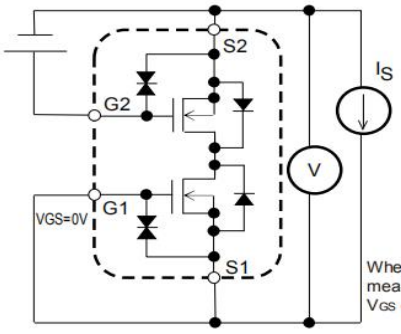
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 6
Qg



When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 7
$V_{F(S-S)}$



When FET1 is measured,+4.5V is added to Vgs of FET2.

特征电学和温度曲线 Typical Electrical and Thermal Characteristics

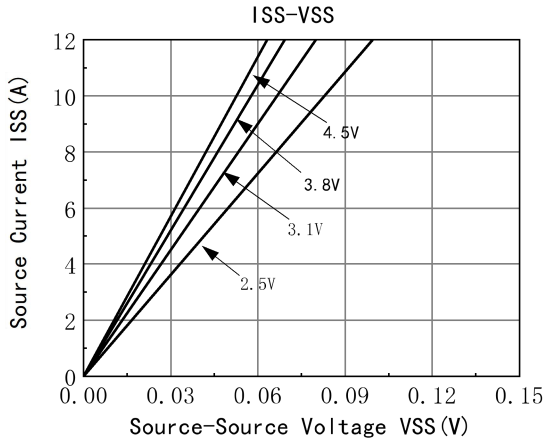


Figure 1: On-Region Characteristics

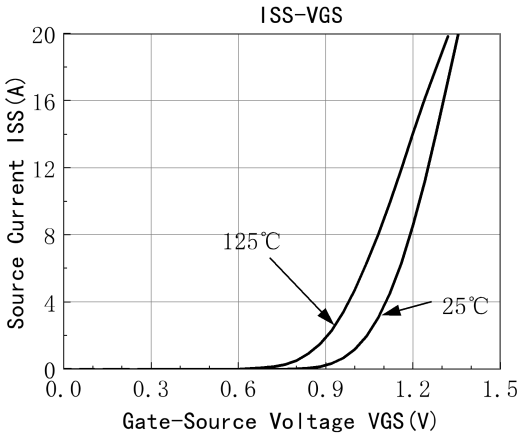


Figure 2: Typical Transfer Characteristics

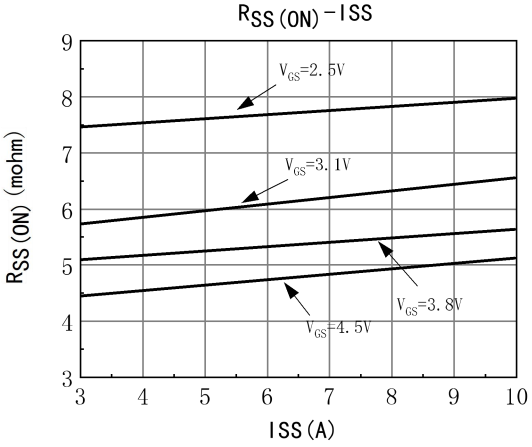


Figure 3: On-Resistance vs. Source Current and Gate Voltage

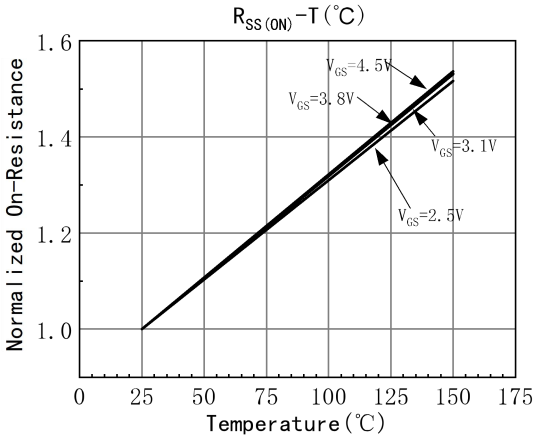


Figure 4: On-Resistance vs. Junction

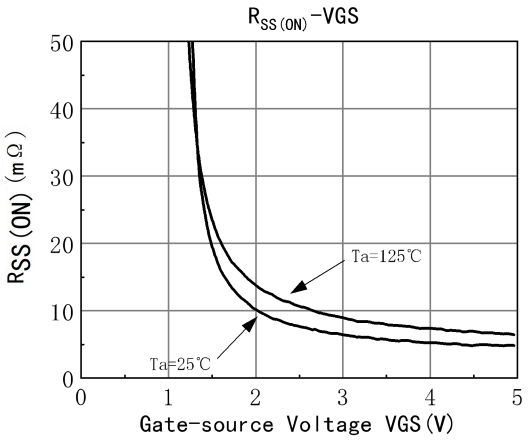


Figure 5: On-Resistance vs. Gate- Source Voltage

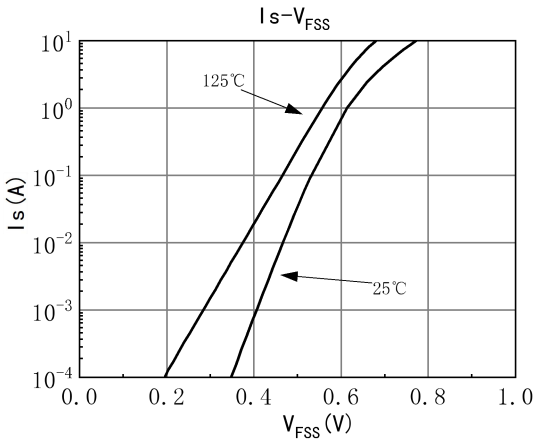
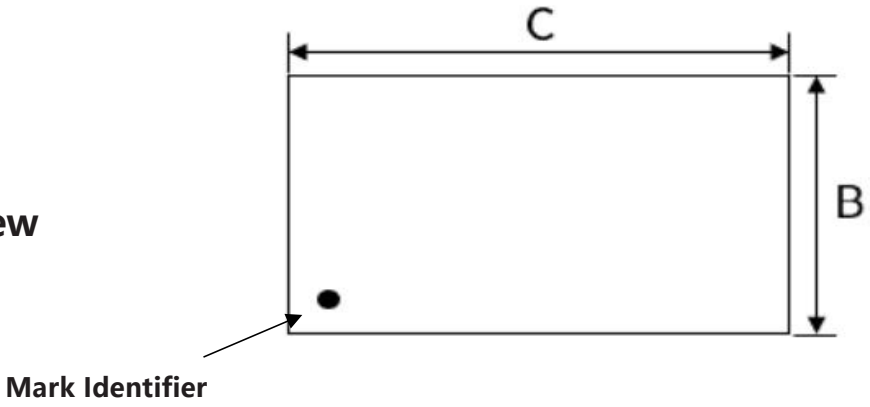


Figure 6: Forward Source to Source Characteristics

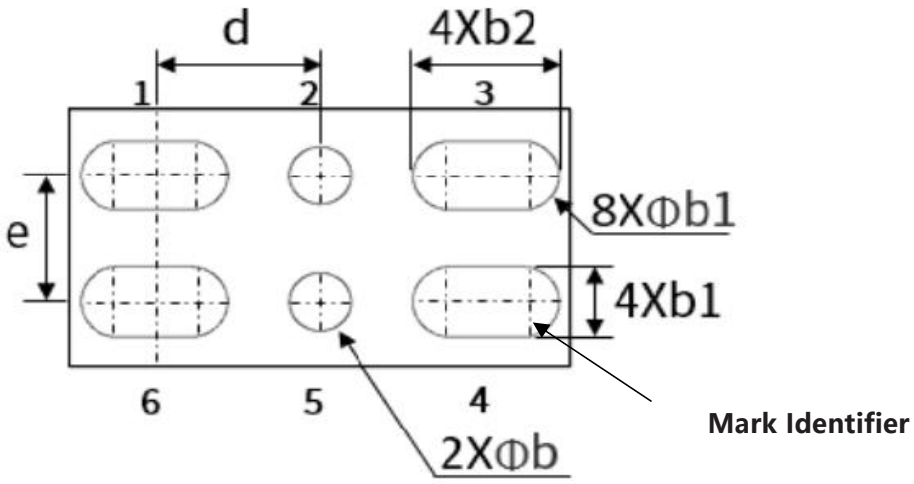
封装尺寸 Package Dimensions

Top View



Side View

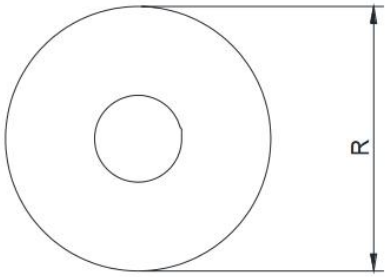
Bottom View



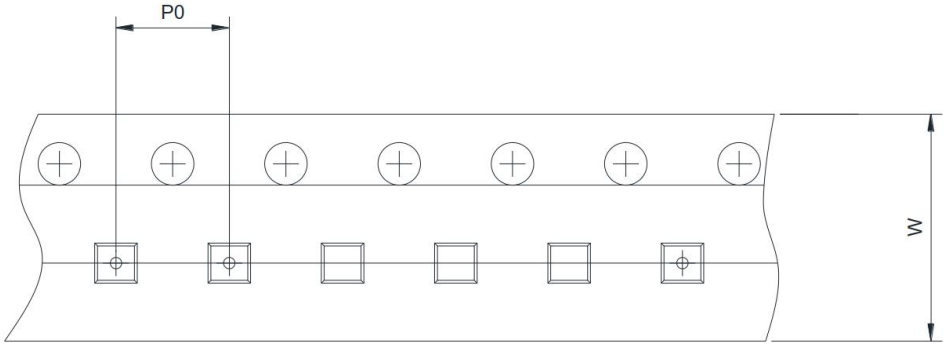
Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.27	0.30	0.33	0.0106	0.0118	0.0130
B	1.12	1.18	1.24	0.0441	0.0465	0.0488
C	2.05	2.11	2.17	0.0807	0.0831	0.0854
b	0.22	0.25	0.28	0.0087	0.0098	0.0110
b1	0.27	0.3	0.33	0.0106	0.0118	0.0130
b2	0.57	0.6	0.63	0.0224	0.0236	0.0248
d	0.6575	0.6775	0.6975	0.0259	0.0267	0.0275
e	0.53	0.55	0.57	0.0209	0.0217	0.0224

载带和卷盘信息 TAPE AND REEL INFORMATION

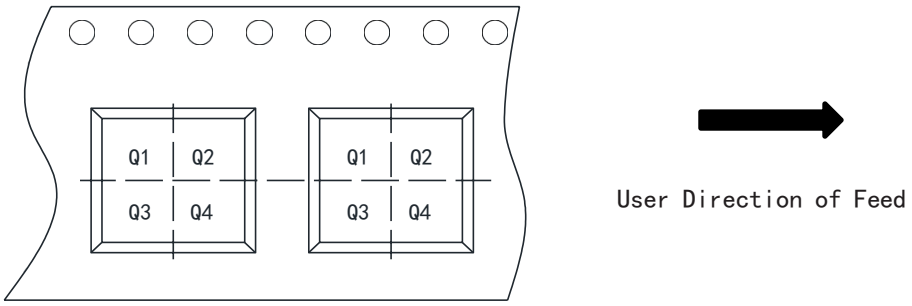
Reel Dimensions



Tape Dimensions

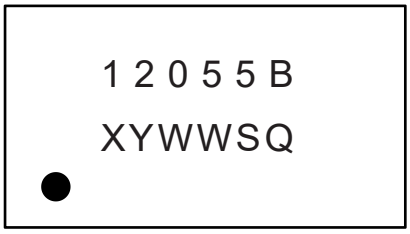


Quadrant Assignments For PIN1 Orientation In Tape



R	Reel Dimension	☑7inch ☐13inch
W	width of the carrier tape	☑8mm ☐12mm
P0	Pitch between successive cavity centers	☐2mm ☑4mm ☐8mm
Pin1	Pin1 Quadrant	☐ Q1 ☐Q2 ☐Q3 ☑Q4

丝印信息 Marking Information



NOTE:	
12055B	Product Code
X	Variable code
Y	Year code
WW	Week code
SQ	Serial NO

历史版本 Version history

版本号	时间	修改内容
V1.0	2025 年 03 月	初始版本
V1.1	2025 年 04 月	更新 VF 典型值，增加载带，丝印说明